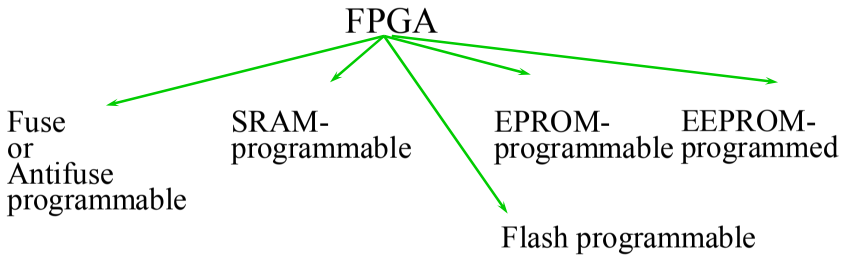
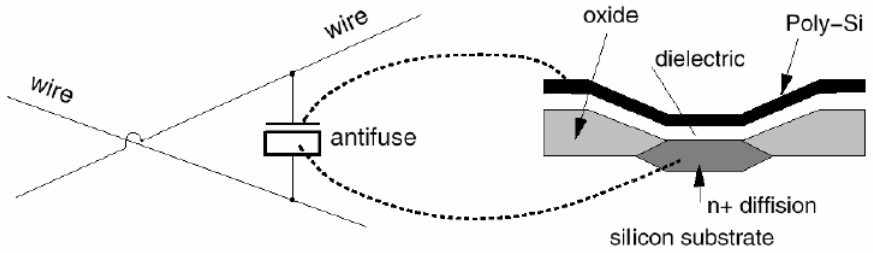
FPGA classified based on the configuration method

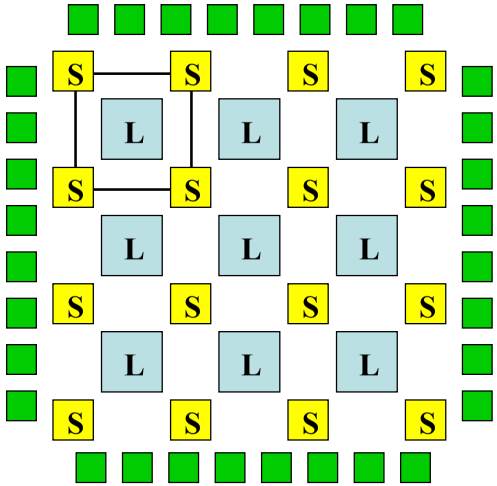


Anti-Fuse based FPGA

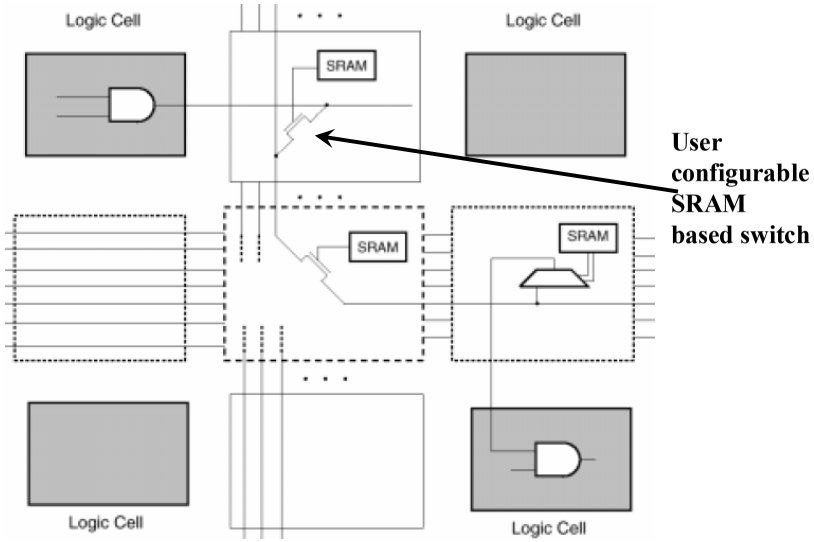


Actel Anti-fuse switch technology

Block organized, SRAM based



SRAM based FPGA



FPGA configuration technologies - comparison

Name	Re-programmable	Volatile	Technology
Fuse	no	no	Bipolar
EPROM	yes out of circuit	no	UVCMOS
EEPROM	yes in circuit	no	EECMOS
SRAM	yes in circuit	yes	CMOS
Antifuse	no	no	CMOS+

SRAM Programming Technology

- Advantages:
  - Reprogrammability
  - Standard process technology.
- Disadvantages:
  - Volatile, hence FPGAs must be reprogrammed each time when power is applied
  - Extra chip area (6 transistors for 1 cell + 1 switch)

Popular FPGAs

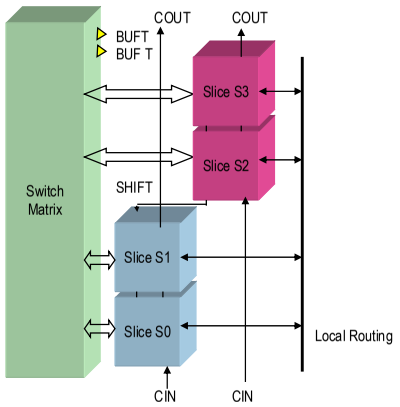
- Xilinx
  - Spartan XL, Spartan II, Spartan 3, Spartan 3E
  - Virtex, Virtex E
  - Virtex II Pro, Virtex 4, Virtex 5
- Altera
  - Cyclone, Cyclone II
  - Stratix, Stratix II, Stratix III
  - Stratix GX, Stratix II GX

Popular FPGAs

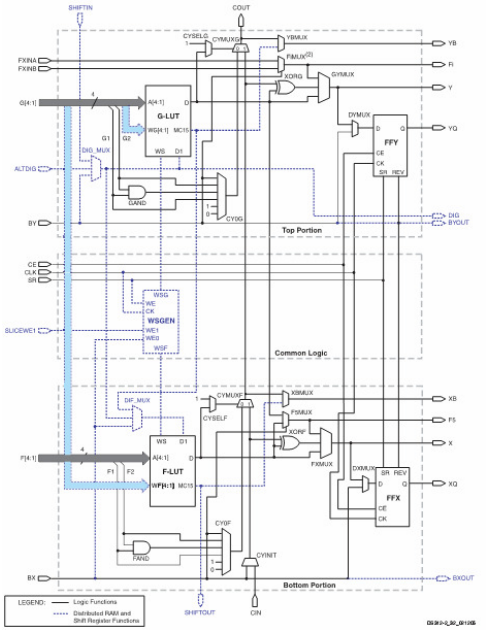
- Actel
  - A54SX-A, Axcelerator (Antifuse)
  - IGLOO, IGLOOE (Flash)
  - ProASIC Plus (Flash)
  - ProASIC3, ProASIC3E (Flash)

Xilinx Spartan 3E CLB

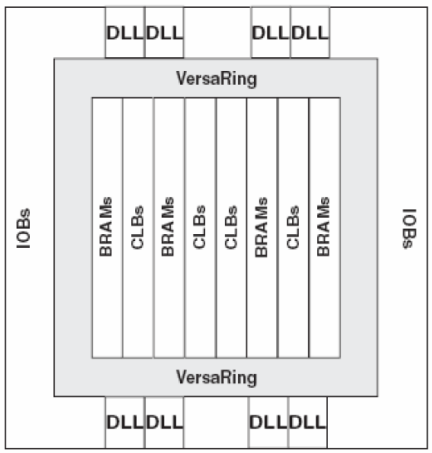
- Each CLB contains four slices
  - Local routing provides feedback between slices in the same CLB, and it provides routing to neighboring CLBs
  - A switch matrix provides access to general routing resources



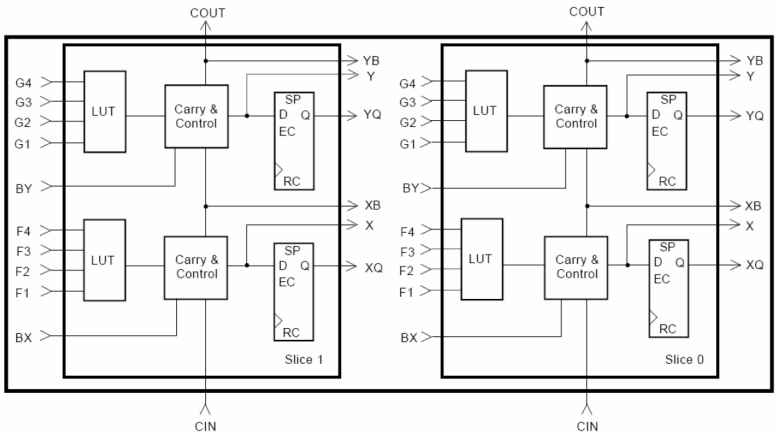
Slice of Xilinx Spartan 3E FPGA



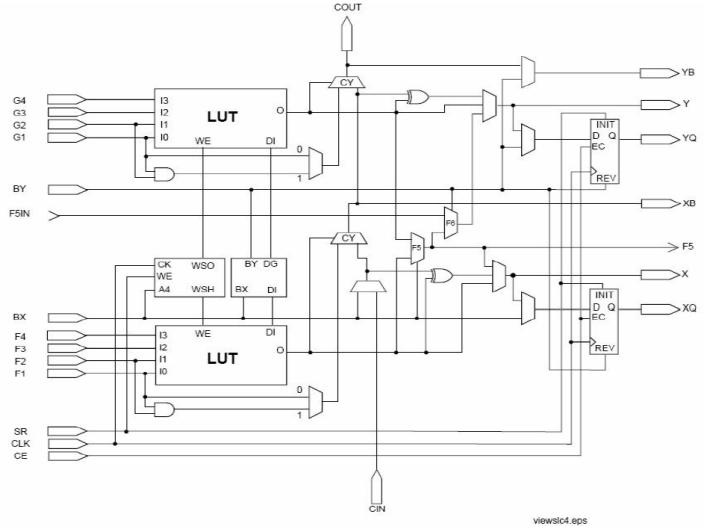
Xilinx Virtex FPGA



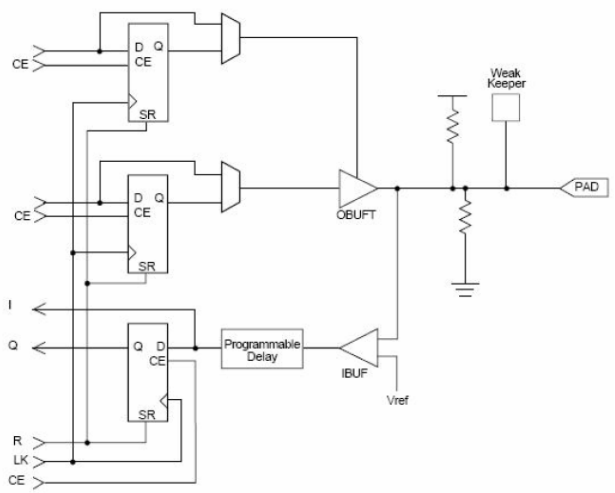
Virtex CLB – 2 slices



Virtex Slice



Virtex IOB



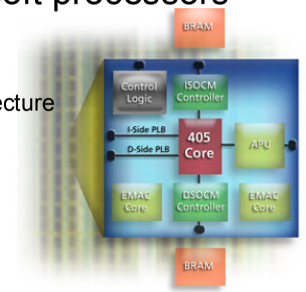
FPGAs to create processor like environment

- Softcore processor
  - The microprocessor (or microcontroller) code is written in VHDL or verilog HDL and downloaded on FPGA.
  - Some FPGA CLB resources are occupied by processor remaining can be used for any other logic

SOC

- Hardcore processor
  - The processor is made on die (on silicon) direclty
  - The processor on die can work like any other normal microprocessor. The surrounding FPGA CLBs can be used for other logic.

Xilinx FPGA with Hard & soft processors

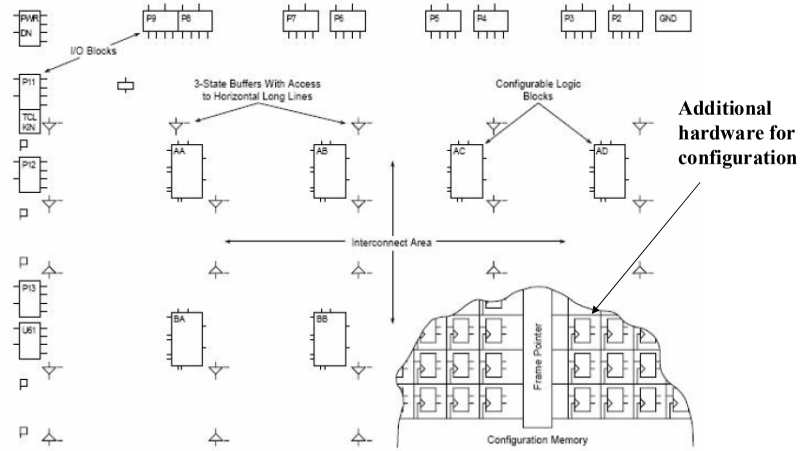


- **PowerPC 405 (hard core)**
  - 32 bit embedded PowerPC RISC architecture
  - Up to 450 MHz
  - 2x 16 kB instruction and data caches
  - Memory management unit (MMU)
  - Hardware multiply and divide
  - Embedded in Virtex-II Pro and Virtex-4
- **MicroBlaze (soft core)**
  - 32 bit RISC architecture
  - 2-64 kB instruction and data caches
  - Barrel Shifter
  - Hardware multiply and divide
  - **OPB** and LMB bus interfaces
- **Others**
  - NIOS softcore (Altera), ARM soft core, PicoBlaze softcore (Xilinx), ...

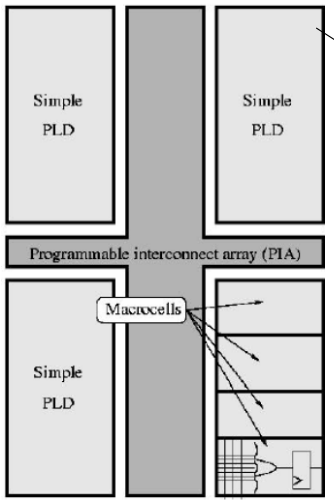
Advantages and Disadvantages of FPGAs (in comparison with ASIC)

- Advantages
  - Fast turnaround.
  - Low NRE (non-recurring engineering) changes.
  - Low risk.
  - Effective design verification.
  - low testing cost.
- Disadvantages
  - Bigger Chip size
  - More unit cost.
  - Slow speed.

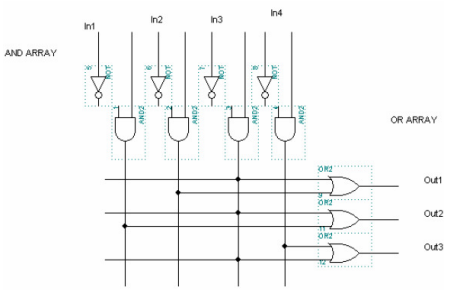
Why FPGA has bigger chip area ? (FPGA - Area overhead)



Complex programmable logic device (CPLD)



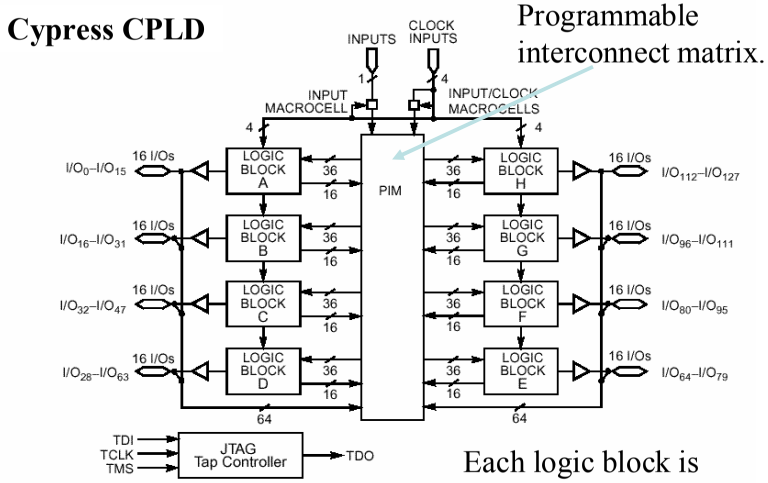
Typically a CPLD consists of 50 SPLDs (An SPLD is a programmable logic array with AND and OR planes)



Programmable Logic Array

Cypress CPLD

Programmable interconnect matrix.



Each logic block is similar to a 22V10.

Figure 1. Ultra37128 Block Diagram

CPLD Vs. FPGA

	CPLD	FPGA
Interconnect style	Continuous	Segmented
Architecture and timing	Predictable	Unpredictable
Software compile times	Short	Long
In-system performance	Fast	Moderate
Applications addressed	small size	smaller size to very big size

FPGA Selection Criteria

- Required Logic Density (gate count)
- Required I/Os
- Required Speed
- Affordable Price
- Package type
- Involved issues in PCB design

Challenges for Future FPGA

- Scalability of design methodology
- Dominance of wire delays
  - Already more than 50% of delay
- Power consumption
- Complex communication patterns
- Prototyping for NoC-based SoCs
- Including analog hardware